WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a gate over a semiconductor region;

forming a first junction by doping an n-type impurity less diffusive than phosphorus in the semiconductor region by using the gate as a mask; and

forming a second junction by doping an n-type impurity in the semiconductor region by using at least the gate as a mask, the second junction being deeper than the first junction, the second junction overlapping with the first junction with leaving a part of the first junction existing under the gate, wherein

the step of forming the first junction includes at least a first ion implantation which is carried out with a first acceleration energy and a first dose, and a second ion implantation which is carried out with a second acceleration energy higher than the first acceleration energy and a second dose lower than the first dose.

2. The method for manufacturing a semiconductor device according to claim 1, wherein

in the step of forming the first junction, arsenic is used as the less diffusive n-type impurity.

3. The method for manufacturing a semiconductor device according to claim 1, wherein

the step of forming the first junction includes a

third ion implantation which is carried out with a third acceleration energy and a third dose, in addition to the first and second ion implantations.

4. The method for manufacturing a semiconductor device according to claim 1, further comprising the step of forming side walls over both sides of the gate, and wherein

the step of forming the second junction is carried out by using the gate and the side walls as a mask.

5. The method for manufacturing a semiconductor device according to claim 1, further comprising the step of processing the gate to take the shape of a notch, and wherein

the step of forming the first junction is carried out by using the gate in the shape of the notch as a mask.

6. The method for manufacturing a semiconductor device according to claim 1, further comprising the step of doping a p-type impurity in the surface layer of the semiconductor region by using the gate as a mask.

7. The method for manufacturing a semiconductor device according to claim 1, wherein

the second ion implantation is carried out with the acceleration energy of 20keV to 30keV and the dose of $1\times10^{13}/cm^2$ to $3\times10^{13}/cm^2$.

8. A semiconductor device comprising a gate, a

source, and a drain, wherein

an n-type impurity less diffusive than phosphorus is doped in the source and the drain, which include a first junction and a second junction, the second junction being deeper than the first junction, the second junction overlapping with the first junction with leaving a part of the first junction existing under the gate, and

in the lower portion of the first junction, a decline region of the concentration of the low diffusive n-type impurity is formed, a width of the decline region expanding with getting near an end of the gate in the inside of the end the gate, and becoming approximately even in the outside of the end the gate.

9. The semiconductor device according to claim 8, wherein

the less diffusive n-type impurity is arsenic.

10. The semiconductor device according to claim 8, further comprising a p-type impurity region formed such that a part of the region overlaps with the source and the drain.